PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)
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Stolowitz, Michael C.	) Art Unit: 2188
	)
Application No. 10/822,115	) Examiner: Walter, Craig E.
	)
Filed: 04/08/2004	) Atty. Docket No.
	) NVIDP486/P003259
For: METHOD AND APPARATUS FOR SYNCHRONIZING DATA FROM ASYNCHRONOUS DISK DRIVE DATA TRANSFERS	)
	) Date: 07/14/2008
	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

REPLY BRIEF (37 C.F.R. § 41.37)

This Reply Brief is being filed within two (2) months of the mailing of the Examiner's Answer mailed on 05/14/2008.

Following is an issue-by-issue reply to the Examiner's Answer.

Issue # 1:

The Examiner has rejected Claim 31 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Group #1: Claim 31

In the Examiner's Answer dated 05/14/2008, the Examiner has withdrawn the rejection of Claim 31 under 35 U.S.C. 112, first paragraph.

Issue # 2:

The Examiner has rejected Claims 12 and 17-25 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appellant regards as the invention.

Group #1: Claims 12 and 17-25

In the Examiner's Answer dated 05/14/2008, the Examiner has withdrawn the rejection of Claims 12 and 17-25 under 35 U.S.C. 112, second paragraph.

Issue # 3:

The Examiner has rejected Claims 1, 3-5, 8, 10-12, 14, 16, 26-28, and 31 under 35 U.S.C. 102(b) as being anticipated by Searby (U.S. Patent No. 5,765,186).

Group #1: Claims 1, 3-5, 8, 10-12, 14, and 16

With respect to independent Claims 1 and 10, the Examiner has relied on Col. 3, lines 52-67 from the Searby reference to make a prior art showing of appellant's claimed "memory for receiving and storing read data responsive to timing signals provided by the respective drive" (see this or similar, but not necessarily identical language in the aforementioned claims).

Appellant respectfully notes that Searby discloses that "[t]he controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40" (Col. 6, line 64 – Col. 7, line 1). In addition, Searby teaches that "[w]hen data is ready for transfer a signal is sent from the interfaces 33 to 36" and that "once the controller has received signals from each of the interfaces it enables data to be transferred between the interfaces and respective RAM buffers" (Abstract).

However, waiting until all of the disc interfaces have data ready before transferring data, as in Searby, does not teach "receiving and storing read data responsive to timing signals provided by the respective drive" (emphasis added), as claimed by appellant. Additionally, "wait[ing] until all... of the second interfaces have output a request signal before outputting a write strobe signal" (emphasis added), as in Searby, fails to disclose "receiving and storing read data responsive to timing signals provided by the respective **drive**" (emphasis added), as claimed.

In the Office Action dated 03/26/2007, the Examiner has argued that "[appellant] does in fact describe synchronizing the data transfer from drives to the buffer," and has further argued that "[appellant] concedes by his own admission that Searby synchronizes data transfer from the drives to the RAM buffer, as similarly recited by [appellant] in the preamble."

Appellant respectfully disagrees and notes that appellant claims "memory for receiving and storing read data responsive to timing signals provided by the respective drive" and "synchronously reading the transferred data from all of the...memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer" (see the same or similar, but not necessarily identical language in independent Claims 1 and 10 - emphasis added), in the context claimed. Thus, Searby's mere disclosure of waiting until all of the disc interfaces have data ready before transferring data fails to meet appellant's specific claim language, namely "memory for receiving read data responsive to timing signals provided by the respective drive" in addition to "synchronously reading the transferred data from all of the...memories" (emphasis added), in the context claimed.

In addition, the excerpts relied on by the Examiner merely teach "transferring means comprising means for providing an indication when said data is available for transfer" and that "the controlling means [are] responsive to said indication from said transferring means" (Col. 3, line 59 – Col. 4, line 1 – emphasis added). However, merely disclosing controlling means responsive to an indication from a transferring means that data is available for transfer, as in Searby, does not teach "receiving and storing read data responsive to timing signals provided by the respective drive" (emphasis added), as claimed by appellant. Clearly, an indication from transferring means that data is available for transfer, as in Searby, simply fails to even suggest "timing signals provided by the respective drive" (emphasis added), in the manner as claimed by appellant.

In the Examiner's Answer dated 05/14/2008, the Examiner has argued that "the point [of] contention... is whether or not the request signals utilized by the drives via their respective interfaces in fact constitutes 'timing signals provided by the respective drive[s].'" Additionally, the Examiner has referred to "the previously cited [reference (] col. 5, ll. 38-49) [where the] Examiner clearly mapped each of the drive's associated respective signals, to Appellant's timing information (see also Examiner response to arguments in the Office action made FINAL 26 March 2007 – page 20, ll. 1-7)." Further, the Examiner has argued that "in Searby, it is the controller that in fact waits on each drive's respective SCSI interfaces to output their respective signals until the data is transferred to each of their respective RAMs (see col. 6, l. 59 through col. 7, l. 9)" and has additionally argued that "this 'waiting' for an outputted request as disclosed by Searby is in fact necessary for data to be properly transferred from each drive to its respective RAM, and further constitutes 'timing information' because the request is used for the express purpose of ensur[ing] data synchronization via correct timing." The Examiner has also argued that "[e]ach drive's SCSI interface is merely a conduit for each of the drive's data and control information, [and] therefore these requests (e.g., timing information) must in fact be 'provided by' each drive."

Appellant respectfully disagrees. First, appellant notes that the excerpts relied on by the Examiner merely teach that "a system controller... receives frame request data from an external processing apparatus... via request bus 52 and in response thereto outputs control data" (Col. 5, lines 39-42 – emphasis added), and that "[t]he controller 51 also receives request signals REQ from each of the second SCSI interfaces... associated with the RAM buffers... thereby controlling the outputting of data" (Col. 5, lines 44-49 – emphasis added). Additionally, appellant again notes that the excerpts

teach that "[t]he controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40" (Col. 6, line 64 – Col. 7, line 1).

However, receiving request signals from SCSI interfaces associated with RAM buffers which controls the output of data, as in Searby, does not disclose that "these requests (e.g., timing information) must in fact be 'provided by' each drive," as argued by the Examiner, and does not teach "memory for receiving and storing read data responsive to **timing signals** provided by the **respective drive**" (emphasis added), as claimed by appellant. Additionally, waiting until all of the disc interfaces have data ready before transferring data, as in Searby, does not "constitut[e] 'timing information'," as argued by the Examiner, and also fails to teach "receiving and storing read data responsive to **timing signals** provided by the **respective drive**" (emphasis added), as claimed by appellant. Furthermore, "wait[ing] until all... of the second interfaces have output a request signal before outputting a write strobe signal" (emphasis added), as in Searby, fails to disclose "receiving and storing read data responsive to timing signals provided by the **respective drive**" (emphasis added), as claimed.

Additionally, with respect to the Examiner's allegation that "[e]ach drive's SCSI interface is merely a conduit for each of the drive's data and control information, [and] therefore these requests (e.g., timing information) must in fact be 'provided by' each drive," it appears that the Examiner has relied on an inherency argument regarding the above emphasized claim limitations. Appellant respectfully asserts that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

In view of the arguments made hereinabove, any inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested. (See MPEP 2112)

In addition, with respect to independent Claims 1 and 10, the Examiner has relied on Col. 5, lines 38-49 from the Searby reference to make a prior art showing of appellant's claimed "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive" (see this or similar, but not necessarily identical language in the aforementioned claims).

Appellant again notes that merely waiting until all of the disc interfaces have data ready before transferring data, as in Searby, does not teach "transfer[ring] the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive" (emphasis added), as claimed by appellant. Additionally, "wait[ing] until all... of the second interfaces have output a request signal before outputting a write strobe signal" (emphasis added), as in Searby, fails to disclose "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective **drive**" (emphasis added), as claimed.

In the Office Action dated 03/26/2007, the Examiner has argued that in "Searby in Fig. 2, and col. 5, lines 39-49, a request signal is associated with each respective drive, in order to control the transfer of information." Appellant respectfully disagrees and notes that the excerpts relied on by the Examiner merely teach that "a system controller... receives frame request data from an external processing apparatus... via request bus 52 and in response thereto outputs control data" (Col. 5, lines 39-42 – emphasis added). In addition, Searby teaches that "[t]he controller 51 also receives request signals REQ from each of the second SCSI interfaces... associated with the RAM buffers... thereby controlling the outputting of data" (Col. 5, lines 44-49 – emphasis added). However, receiving request signals which control the output of data, as in Searby, does not teach "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the **timing signals** provided by the **respective drive**" (emphasis added), as claimed by appellant. Clearly, receiving request signals from each of the second SCSI interfaces, as in

Searby, simply fails to even suggest "timing signals provided by the respective drive" (emphasis added), in the manner as claimed by appellant.

In the Examiner's Answer dated 05/14/2008, the Examiner has again relied on Col. 5, lines 38-49 and Col. 6, line 59-Col. 7, line 9 of Searby, and has again argued that "[the controller] 'waiting' for an outputted request as disclosed by Searby is in fact necessary for data to be properly transferred from each drive to its respective RAM, and further constitutes 'timing information' because the request is used for the express purpose of ensur[ing] data synchronization via correct timing." The Examiner has also argued that "[e]ach drive's SCSI interface is merely a conduit for each of the drive's data and control information, [and] therefore these requests (e.g., timing information) must in fact be 'provided by' each drive."

Appellant again respectfully disagrees and notes that the excerpts relied on by the Examiner merely teach that "a system controller... receives frame request data from an external processing apparatus... via request bus 52 and in response thereto outputs control data" (Col. 5, lines 39-42 – emphasis added), and that "[t]he controller 51 also receives request signals REQ from each of the second SCSI interfaces... associated with the RAM buffers... thereby controlling the outputting of data" (Col. 5, lines 44-49 – emphasis added). Additionally, appellant again notes that the excerpts teach that "[t]he controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40" (Col. 6, line 64 – Col. 7, line 1).

However, receiving request signals from SCSI interfaces associated with RAM buffers which controls the output of data, as in Searby, does not disclose that "these requests (e.g., timing information) must in fact be 'provided by' each drive," as argued by the Examiner, and does not teach "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the **timing signals** provided by the **respective drive**" (emphasis added), as claimed by appellant. Additionally, waiting until all of the disc interfaces have data ready before transferring data, as in Searby, does not "constitut[e] 'timing information'," as argued by the Examiner, and also fails to teach "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the **timing signals** provided by the **respective drive**" (emphasis added), as claimed by appellant. Furthermore,

"wait[ing] until all... of the second interfaces have output a request signal before outputting a write strobe signal" (emphasis added), as in Searby, fails to disclose "causing each of the drives to... transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the **respective drive**" (emphasis added), as claimed.

Additionally, based on the Examiner's above noted argument, it again appears that the Examiner has relied on an inherency argument regarding the above emphasized claim limitations. In view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested (See MPEP 2112). Also, see *In re Rijckaert* , *In re Oelrich*, and *In re Robertson* hereinabove.

Further, with respect to independent Claims 1 and 10, the Examiner has relied on Fig. 2, element 49 and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "monitoring each of the two-port memories to detect a non-empty condition" (see this or similar, but not necessarily identical language in the aforementioned claims).

More specifically, in the Office Action dated 07/13/2006, the Examiner argued that Searby "transfers the data to the data highway...based on the determination that data is stored in the RAM buffers." Further, the Examiner argued that "[s]ince all the buffers receive data substantially concurrently (i.e., all disk stores send data to the RAM buffers at the same time, which causes either all the buffers to contain data, or no buffers to contain data), each RAM is monitored to determine that data is either present (i.e., non-empty condition), or not present." In addition, the Examiner argued that "[d]ata present in the RAM buffers is an implied acknowledgement that data have been received from the disk stores" and that "the system cannot transfer data to the highway until data is present in the RAM buffers; therefore the memories are monitored for this determination to occur."

Appellant disagrees and again respectfully notes that Searby discloses that "[t]he controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40" (Col. 6, line 64 – Col. 7, line 1). Further, Searby teaches that "[a]t the same time, the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data

from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, lines 3-7).

However, merely writing data into all of the RAM buffers using a common strobe signal, in addition to providing RAM addressing, as taught in Searby, fails to disclose "monitoring each of the two-port memories to detect a non-empty condition" (emphasis added), as claimed by appellant. More specifically, because the controller in Searby itself effects the writes to the RAM buffers, it "knows" when they have received data from the drives. Further, as all of the RAMs receive data concurrently, monitoring any one of them would suffice to determine its status. Since the process in Searby is all synchronous, the controller has no need to "monito[r] each of the two-port memories to detect a non-empty condition" (emphasis added), as claimed.

In the Office Action dated 03/26/2007, the Examiner has relied on an inherency argument regarding appellant's claimed "monitoring each of the two-port memories to detect a non-empty condition," as claimed. Specifically, the Examiner has argued that "memory monitoring to some degree is inherent in a system such as Searby's." because" "Searby's system is directed to the parallel transfer of data, [such that] the system must wait until each of the memories has data present before the data can be sent to the highway." The Examiner has thus concluded that, "[Searby's] system must inherently perform some sort of monitoring process of the memories to determine if data is present to transfer."

Appellant respectfully disagrees and asserts that Searby merely discloses that "[t]he registers 41 to 44 each hold a single word of data and the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence" and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49" (Col. 7, lines 39-42 – emphasis added). However, merely enabling a tri-state buffer for output of the data word from the respective register, as in Searby, simply fails to even suggest "monitoring each of the two-port memories to detect a non-empty condition" (emphasis added), as claimed. In view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested. (See MPEP 2112)

Additionally, in response, appellant asserts that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

In the Examiner's Answer dated 05/14/2008, the Examiner has argued that "[a]ppellant fails to address critical lines of Searby relied upon by Examiner to form the rejection (namely, col. 7, ll. 32-38 – these lines clearly disclose that data in the RAM can be outputted only when data is in all RAM buffers (e.g. non-empty condition))." The Examiner has also argued that "memory monitoring is inherent in a system such as Searby's" since "before Searby's system is capable of transferring data to the data highway and ultimately to the buffer (col. 7, lines 32-35), the system must in fact determine that data is stored in each of the buffers (since Searby's system is directed to the parallel transfer of data, the system must wait until each of the memories has data present before the data can be sent to the highway)." Additionally, the Examiner has argued that "[a] system of Searby's would clearly not be enabled if it were not cognizant of data stored in each of its RAM buffers, hence this 'monitoring' is in fact inherent." Further, the Examiner has argued that "Searby must wait until data is present before it can be stored" and that "therefore, his system must inherently perform some sort of monitoring process of the memories to determine if data is present to transfer (i.e. non-empty condition)." Further still the Examiner has argued that since the "Examiner has no intrinsic evidence from [appellant's] specification to rely upon to further define 'monitoring'," that "[o]ne of ordinary skill in the art would understand 'monitoring' to include 'the observation, detection, or recording of an operation of a machine or system' (standard English dictionary definition)," and that "therefore [the] Examiner has properly applied this definition against the claims as being the 'broadest reasonable interpretation consistent with [appellant's] specification' pursuant to MPEP § 2111." The Examiner has also argued that "[s]ince Searby's system must inherently observe or detect if data is stored in each memory before said data can be transferred (otherwise the system would be incapable of accessing the data stored therein), Searby in fact anticipates this limitation."

Appellant respectfully disagrees. First, appellant respectfully notes that the aforementioned claim language is to be read according to the plain and ordinary meaning thereof, in view of dictionary definitions, and in further view of the specification. For example, appellant specifically claims "monitoring each of the two-port memories to detect a non-empty condition" (see this or similar, but not necessarily identical language in the aforementioned claims – emphasis added).

Additionally, appellant again respectfully points out that Searby discloses that a "controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40," that "[t]he write strobe signal causes the RAM buffers 37 to 40 to receive a word of data from their respective second SCSI interfaces 33 to 36," and that "[a]t the same time, the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, line 64 – col. 7, line 7 – emphasis added). Additionally, Searby discloses that "[t]his process is repeated until all of the data relating to the requested frame has been copied from the disc stores 21 to 24 to the RAM buffers 37 to 40" and that in one embodiment, "[e]ach sub-controller would monitor the request signal REQ from its second SCSI interface and in response to a request would strobe the write line of its RAM buffer causing a word to be transferred from the second SCSI interface to the RAM buffer" (Col. 7, lines 7-20).

As a result, the excerpt relied on by the Examiner that teaches that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" (Col. 7, lines 32-34), which refers to the repetition of the write strobe signal to the RAM buffers in order to copy all data relating to a requested frame to the RAM buffers. In turn, the write strobe signals are reliant on the controller monitoring request signals from the second SCSI interfaces and determining that all twenty of the second interfaces have output a request signal. As a result, the excerpt relied on by the Examiner merely discloses that data can be output from the RAM to the highway once the repeated monitoring of request signals from the SCSI interfaces and associated outputting of write strobe signals to the RAM buffers has been performed for all data in a requested frame.

However, merely monitoring request signals from the SCSI interfaces, in addition to outputting write strobe signals to RAM buffers once all SCSI interfaces have output a request signal, as in Searby, does not disclose "monitoring each of the two-port memories to detect a non-empty condition" (emphasis added), as claimed by appellant.

Additionally, with respect to the Examiner's aforementioned inherency argument regarding the above emphasized claim limitations, appellant respectfully notes that in view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested (See MPEP 2112). Also, see *In re Rijckaert* , *In re Oelrich*, and *In re Robertson* hereinabove.

In the Examiner's Answer dated 05/14/2008, the Examiner has additionally argued that with respect to "whether or not Searby's system 'waits' until all two-port memories are 'non-empty' prior to outputting the data... Examiner again points to the cited lines not contemplated by [a]ppellant when addressing Examiner's rejection (col. 7, ll. 32-38) which clearly describe waiting for data to be present in all RAMs prior to transmission." The Examiner has further argued that "[t]he lines additional[ly] address [a]ppellant's concern that only one RAM would be monitored if data is transferred to them (system must wait until data is present in all RAMs)."

Appellant respectfully disagrees and again notes that the excerpt relied on by the Examiner merely discloses that data can be output from the RAM to the highway once the repeated monitoring of request signals from the SCSI interfaces and associated outputting of write strobe signals to the RAM buffers has been performed for all data in a requested frame. Again, merely monitoring request signals from the SCSI interfaces, in addition to outputting write strobe signals to RAM buffers once all SCSI interfaces have output a request signal, as in Searby, does not disclose "monitoring each of the two-port memories to detect a non-empty condition" (emphasis added), as claimed by appellant.

Additionally, appellant again notes that because the controller in Searby itself effects the writes to the RAM buffers by outputting the write strobe signals, it "knows" when they have received data from the drives. Further, as all of the RAMs receive data concurrently as a result of the write strobe,

monitoring any one of them would suffice to determine its status. Since the process in Searby is all synchronous, the controller has no need to "monito[r] each of the two-port memories to detect a non-empty condition" (emphasis added), as claimed.

Further, with respect to independent Claims 1 and 10, the Examiner has relied on Fig. 2, elements 49 and 50; Col. 5, lines 22-37; Col. 6, lines 14-31; and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer" (see this or similar, but not necessarily identical language in the aforementioned claims).

Appellant respectfully notes that Searby discloses that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" and that "[d]ata is output from the RAM buffers 37 to 40 by applying a read strobe signal to the line 54 while simultaneously addressing the same location in each of the stores" (Col. 7, lines 32-37). In addition, as mentioned above, Searby teaches that "the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, lines 3-7). However, merely waiting to collect a full frame of data, where the data was already synchronized as it was written into the RAM buffer, as noted above, fails to disclose "synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer" (emphasis added), as claimed by appellant.

In the Office Action dated 03/26/2007, the Examiner has argued that "synchronous data is formed and written at least by the time it is transmitted, hence Searby does in fact [teach] 'synchronously reading the transferred data from all of the two-port memories'" and that "therefore the data *formed* from this transmission is in fact synchronous as required by the instant claim." Appellant respectfully disagrees and notes that the excerpts from Searby relied on by the Examiner merely teach that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway" (Col. 7, lines 32-34) where "the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence" and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway

49" (Col. 7, lines 40-42 – emphasis added). However, the mere disclosure that the word is output as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest "forming synchronous read data" by "synchronously reading the transferred data from all of the two-port memories" (emphasis added), as claimed by appellant.

In the Examiner's Answer dated 05/14/2008, the Examiner has argued that "the entire purpose of Searby is to synchronize and buffer image data for parallel and concurrent data transfer (abstract and col. 4, ll. 11-28)." Additionally, the Examiner has argued that "[r]eferring again to col. [8], ll. 32-35, by 'waiting' until all RAMs contain data, and transmitting data from all RAM concurrently, Searby is in fact 'forming synchronous read data' and 'reading [said] data from all of the two-port memories' as required by the claim."

Appellant respectfully disagrees and notes that the excerpts relied on by the Examiner merely disclose that "each of the random access buffers [is] interfaced to a sequential data highway and [is] controlled by the controller such that data can be transferred substantially continuously when required in a controlled sequence between the buffers and the highway" (Col. 4, lines 24-28) and that "once the controller has received signals from each of the interfaces it enables data to be transferred between the interfaces and respective RAM buffers" where "[a] data highway 49 is provided for connection to external apparatus for a substantially continuous sequential transfer of the data in the identified set or all of the identified sets" (Abstract). Further, the excerpts disclose that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" and that "[d]ata is output from the RAM buffers 37 to 40 by applying a read strobe signal to the line 54 while simultaneously addressing the same location in each of the stores (Col. 7, lines 32-37). Additionally, appellant again notes that Searby discloses that "[t]his causes one stored word of data to be output from each of the RAM buffers 37 to 40 to the respective register 41 to 44," that "the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence," and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49" (Col. 7, lines 37-42 – emphasis added).

However, merely disclosing that a substantially continuous sequential transfer of data is performed by applying a read strobe to the RAM buffers, where each RAM buffer contains a word of data, and where the word is output from each RAM buffer as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest "synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer" (emphasis added), as claimed by appellant.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the above reference, as noted above.

Group #2: Claims 26-28, and 31

With respect to independent Claim 26, the Examiner has relied on Fig. 2, element 49 and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "monitoring each of the two-port memories to detect a non-full condition."

Appellant respectfully notes that the excerpts from Searby relied on by the Examiner merely teach that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway" (Col. 7, lines 32-34). However, merely teaching that data for a requested frame is output from the RAM buffers once it has all been transferred, as in Searby, does not teach "monitoring each of the two-port memories to detect a **non-full** condition" (emphasis added), as claimed by appellant.

In the Examiner's Answer dated 05/14/2008, the Examiner has argued that "[a]ppellant's arguments are identical to those set forth under Issue #3, Group #1, Argument #2" and that "therefore those

arguments are not persuasive for the reasons stated by the Examiner under that heading, *supra*." With respect to the reasons referred to by the Examiner, appellant again notes that the Examiner has argued that "[a]ppellant fails to address critical lines of Searby relied upon by Examiner to form the rejection (namely, col. 7, ll. 32-38 – these lines clearly disclose that data in the RAM can be outputted only when data is in all RAM buffers (e.g. non-empty condition))." The Examiner has also argued that "memory monitoring is inherent in a system such as Searby's" since "before Searby's system is capable of transferring data to the data highway and ultimately to the buffer (col. 7, lines 32-35), the system must in fact determine that data is stored in each of the buffers (since Searby's system is directed to the parallel transfer of data, the system must wait until each of the memories has data present before the data can be sent to the highway)." Additionally, the Examiner has argued that "[a] system of Searby's would clearly not be enabled if it were not cognizant of data stored in each of its RAM buffers, hence this 'monitoring' is in fact inherent." Further, the Examiner has argued that "Searby must wait until data is present before it can be stored" and that "therefore, his system must inherently perform some sort of monitoring process of the memories to determine if data is present to transfer (i.e. non-empty condition)." Further still the Examiner has argued that "Examiner has no intrinsic evidence from [appellant's] specification to rely upon to further define 'monitoring'," that "[o]ne of ordinary skill in the art would understand 'monitoring' to include 'the observation, detection, or recording of an operation of a machine or system' (standard English dictionary definition)," and that "therefore Examiner has properly applied this definition against the claims as being the 'broadest reasonable interpretation consistent with [appellant's] specification' pursuant to MPEP § 2111." The Examiner has also argued that "[s]ince Searby's system must inherently observe or detect if data is stored in each memory before said data can be transferred (otherwise the system would be incapable of accessing the data stored therein), Searby in fact anticipates this limitation."

Appellant respectfully disagrees. First, appellant respectfully asserts that appellant claims "monitoring each of the two-port memories to detect a **non-full** condition" (see this or similar, but not necessarily identical language in the aforementioned claims – emphasis added), the above presented arguments for which are clearly not "identical to those set forth under Issue #3, Group #1, Argument #2," as suggested by the Examiner. Second, appellant respectfully notes that the aforementioned claim language is to be read according to the plain and ordinary meaning thereof, in view of dictionary definitions, and in further view of the specification.

Additionally, appellant again respectfully points out that Searby discloses that a "controller 51 is arranged to utilise the buffering provided by the SCSI interface and to wait until all twenty of the second interfaces have output a request signal before outputting a write strobe signal over line 54 to the RAM buffers 37 to 40," that "[t]he write strobe signal causes the RAM buffers 37 to 40 to receive a word of data from their respective second SCSI interfaces 33 to 36," and that "[a]t the same time, the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, line 64 – col. 7, line 7 – emphasis added). Additionally, Searby discloses that "[t]his process is repeated until all of the data relating to the requested frame has been copied from the disc stores 21 to 24 to the RAM buffers 37 to 40" and that in one embodiment, "[e]ach sub-controller would monitor the request signal REQ from its second SCSI interface and in response to a request would strobe the write line of its RAM buffer causing a word to be transferred from the second SCSI interface to the RAM buffer" (Col. 7, lines 7-20).

As a result, the excerpt relied on by the Examiner that teaches that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" (Col. 7, lines 32-34) refers to the repetition of the write strobe signal to the RAM buffers in order to copy all data relating to a requested frame to the RAM buffers. In turn, the write strobe signals are reliant on the controller monitoring request signals from the second SCSI interfaces and determining that all twenty of the second interfaces have output a request signal. As a result, the excerpt relied on by the Examiner merely discloses that data can be output from the RAM to the highway once the repeated monitoring of request signals from the SCSI interfaces and associated outputting of write strobe signals to the RAM buffers has been performed for all data in a requested frame.

However, merely monitoring request signals from the SCSI interfaces, in addition to outputting write strobe signals to RAM buffers once all SCSI interfaces have output a request signal, as in Searby, does not disclose "monitoring each of the two-port memories to detect a **non-full** condition" (emphasis added), as claimed by appellant.

Additionally, with respect to the Examiner's aforementioned inherency argument regarding the above emphasized claim limitations, appellant respectfully notes that in view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested (See MPEP 2112). Also, see *In re Rijckaert* , *In re Oelrich*, and *In re Robertson* hereinabove.

In the Examiner's Answer dated 05/14/2008, the Examiner has additionally argued that with respect to "whether or not Searby's system 'waits' until all two-port memories are 'non-empty' prior to outputting the data... Examiner again points to the cited lines not contemplated by [a]ppellant when addressing Examiner's rejection (col. 7, ll. 32-38) which clearly describe waiting for data to be present in all RAMs prior to transmission." The Examiner has further argued that "[t]he lines additional[ly] address [a]ppellant's concern that only one RAM would be monitored if data is transferred to them (system must wait until data is present in all RAMs)."

Appellant respectfully disagrees. Again, appellant respectfully points out that appellant specifically claims "monitoring each of the two-port memories to detect a **non-full** condition" (see this or similar, but not necessarily identical language in the aforementioned claims – emphasis added). Additionally, appellant again notes that the excerpt relied on by the Examiner merely discloses that data can be output from the RAM to the highway once the repeated monitoring of request signals from the SCSI interfaces and associated outputting of write strobe signals to the RAM buffers has been performed for all data in a requested frame. Again, merely monitoring request signals from the SCSI interfaces, in addition to outputting write strobe signals to RAM buffers once all SCSI interfaces have output a request signal, as in Searby, does not disclose "monitoring each of the two-port memories to detect a **non-full** condition" (emphasis added), as claimed by appellant.

Again, the foregoing anticipation criterion has simply not been met by the above reference, as noted above.

Issue # 4:

The Examiner has rejected Claim 15 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186).

Group #1: Claim 15

In the Office Action dated 03/26/2007, the Examiner has admitted that "Searby does not explicitly teach a method of reading data from an array... wherein each synchronous transfer of read data into the common buffer stores 64-bits of read data," but has argued that "such a limitation is merely a matter of design choice and would have been obvious in the system of Searby." The Examiner has further admitted that "Searby teaches his register (Fig. 2, element 50) as storing information [in] 8-bit format rather than [in] 64-bit as claimed by [appellant]," but has argued that "[t]he fact that Searby differs [from] the claimed invention only by the width of the data stored fails to define a patentably distinct invention over Searby, since both the claimed invention and Searby's teachings are both directed [to] synchronous data transfer[s] from asynchronous devices."

Appellant respectfully disagrees and notes that Searby merely discloses that "[d]ata on the highway 49 is in the form of 16-bit words and is reduced to 8-bit bytes of data by a register 50 before being output from the apparatus for display or processing by an editing or a processing system" (Col. 5, lines 33-37). Further, Searby discloses that "[d]ata is transferred along the SCSI highway a byte (8 bits) at a time" and that "[e]ach second SCSI interface 33 to 36 waits until it has received a word (two bytes) of data and then outputs a request signal REQ to the controller 51" (Col. 6, lines 31-34). Further still, Searby teaches that "[i]ncoming 16-bit words of data from the register 50 are input to the parity generator 55 where they are sequentially processed in an exclusive-or operation to produce a 16-bit parity word" (Col. 9, lines 5-8). Appellant respectfully asserts that the disclosure in Searby that a register reduces 16-bit words to 8-bit portions, that data is transferred 8 bits at a time, that request signals are generated after 2 bytes of data are received, and that 16-bit words are processed clearly demonstrates that it would not be obvious that "each synchronous transfer of read data into the common buffer stores 64-bits of read data" (emphasis added), as claimed by appellant.

It thus appears that with respect to dependent Claim 15, the Examiner has simply dismissed the same under Official Notice. Appellant respectfully disagrees for the aforementioned reasons, and formally requests a specific showing of the subject matter in ALL of the claims in any future action. Note excerpt from MPEP below.

"If the [appellant] traverses such an [Official Notice] assertion the examiner should cite a reference in support of his or her position." See MPEP 2144.03.

In the Examiner's Answer dated 05/14/2008, the Examiner has failed to address appellant's above arguments with respect to the aforementioned claim language and has instead argued that the "obviousness rejection asserted by the Examiner was NOT in fact traversed by [a]ppellant in response to the non-final action mailed 13 July 2006." Additionally, the Examiner has argued that "[a]ppellant explicitly conceded that claim 15 is not in fact, by itself, independently patentable ('Applicant does not contend that claim 15 is independently patentable; it is patentable for the reasons explained above with regard to claim 10, as amended – see Applicant's remarks, 14 January 2007)." Further, the Examiner has argued that "[s]ince [a]ppellant explicitly conceded that claim 15 is NOT independently patentable, and he or she did not traverse this Official notice while the application was under non-final rejection, this limitation is in fact considered admitted prior art pursuant to MPEP § 2144.03 (paragraph C)."

Appellant respectfully disagrees and notes that in the Amendment dated 01/14/2007, appellant stated that "claim 15... is patentable for the reasons explained above with regard to claim 10" (see section B, p. 17 – emphasis added). Additionally, appellant respectfully points out that the portion of the MPEP relied on by the Examiner states that "[i]f applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate" (MPEP § 2144.03(C) – emphasis added). Appellant respectfully notes that the Examiner failed to provide such an indication, and instead argued in the Office Action dated 03/26/2007 that "[a]pplicant's arguments with respect to all claims previously rejected under 35 USC 103(a) (i.e. sections B through E of Applicant's remarks – page 17) as being allowable for depending upon a[n] allegedly allowable base claim [are] rendered moot, and Examiner maintains that all base claims remain either anticipated or rendered obvious per the rejections and arguments set forth *supra*" (Page 22 – emphasis added).

Again, appellant respectfully notes that the disclosure in Searby that a register reduces 16-bit words to 8-bit portions, that data is transferred 8 bits at a time, that request signals are generated after 2

bytes of data are received, and that 16-bit words are processed clearly demonstrates that it would not be obvious that "each synchronous transfer of read data into the common buffer stores 64-bits of read data" (emphasis added), as claimed by appellant.

As mentioned above, it appears that with respect to dependent Claim 15, the Examiner has simply dismissed the same under Official Notice. Appellant again respectfully disagrees for the aforementioned reasons, and formally requests a specific showing of the subject matter in ALL of the claims in any future action. Note the applicable excerpt from MPEP above.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on [appellant's] disclosure. *In re Vaeck*,947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above.

Issue # 5:

The Examiner has rejected Claims 6, 7, 13, 29, and 30 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Anderson (U.S. Patent Publication No. 2003/0200478 A1).

Group #1: Claims 6, 7, and 13

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #3, Group #1.

Group #2: Claims 29 and 30

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #3, Group #2.

Issue # 6:

The Examiner has rejected Claims 2, 9, 17, and 19-25 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Stolowitz (U.S. Patent No. 6,018,778).

Group #1: Claims 2 and 9

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #3, Group #1.

Group #2: Claims 17 and 19-25

Further, with respect to independent Claim 17, the Examiner has relied on Fig. 2, elements 49 and 50; Col. 5, lines 22-37; Col. 6, lines 14-31; and Col. 7, lines 32-46 from the Searby reference to make a prior art showing of appellant's claimed "synchronously reading data from all of the two-port memories only when all of the two-port memories have data stored therein, thereby forming synchronous read data."

Appellant respectfully notes that Searby discloses that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" and that "[d]ata is output from the RAM buffers 37 to 40 by applying a read strobe signal to the line 54 while simultaneously addressing the same location in each of the stores" (Col. 7, lines 32-37). In addition, as mentioned above, Searby teaches that "the controller 51 outputs RAM address data to the RAM buffers 37 to 40 so that the data from the second SCSI interfaces 33 to 36 is stored at the same respective locations in the RAM buffers 37 to 40" (Col. 6, lines 3-7). However, merely waiting to collect a full frame of video data, where the data was already synchronized as it was

written into the RAM buffer, fails to disclose "synchronously reading data from all of the two-port memories...thereby forming synchronous read data" (emphasis added), as claimed by appellant.

In the Office Action dated 03/26/2007, the Examiner has argued that "synchronous data is formed and written at least by the time it is transmitted, hence Searby does in fact [teach] 'synchronously reading the transferred data from all of the two-port memories'" and that "therefore the data *formed* from this transmission is in fact synchronous as required by the instant claim." Appellant respectfully disagrees and notes that the excerpts from Searby relied on by the Examiner merely teach that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers... it can be output therefrom to the highway" (Col. 7, lines 32-34) where "the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence" and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49" (Col. 7, lines 40-42 – emphasis added). However, the mere disclosure that the word is output as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest "forming synchronous read data" by "synchronously reading data from all of the two-port memories" (emphasis added), as claimed by appellant.

In the Examiner's Answer dated 05/14/2008, the Examiner has argued that "[a]ppellant's arguments are identical to those set forth under Issue #3, Group #2, Argument #3" and that "therefore those arguments are not persuasive for the reasons stated by the Examiner under that heading, *supra*." With respect to the reasons referred to by the Examiner, appellant again notes that the Examiner has argued that "the entire purpose of Searby is to synchronize and buffer image data for parallel and concurrent data transfer (abstract and col. 4, ll. 11-28)." Additionally, the Examiner has argued that "[r]eferring again to col. [8], ll. 32-35, by 'waiting' until all RAMs contain data, and transmitting data from all RAM concurrently, Searby is in fact 'forming synchronous read data' and 'reading [said] data from all of the two-port memories' as required by the claim."

Appellant respectfully disagrees and notes that the excerpts relied on by the Examiner merely disclose that "each of the random access buffers [is] interfaced to a sequential data highway and [is] controlled by the controller such that data can be transferred substantially continuously when required in a controlled sequence between the buffers and the highway" (Col. 4, lines 24-28) and that "once the controller has received signals from each of the interfaces it enables data to be

transferred between the interfaces and respective RAM buffers" where "[a] data highway 49 is provided for connection to external apparatus for a substantially continuous sequential transfer of the data in the identified set or all of the identified sets" (Abstract). Further, the excerpts disclose that "[o]nce all of the data for the requested frame has been transferred to the RAM buffers 37 to 40 it can be output therefrom to the highway 49" and that "[d]ata is output from the RAM buffers 37 to 40 by applying a read strobe signal to the line 54 while simultaneously addressing the same location in each of the stores (Col. 7, lines 32-37). Additionally, appellant again notes that Searby discloses that "[t]his causes one stored word of data to be output from each of the RAM buffers 37 to 40 to the respective register 41 to 44," that "the word is output therefrom as each of the tri-state buffers 45 to 48 is enabled in sequence," and that "[e]ach tri-state buffer 45 to 48 is enabled individually for output of the data word from the respective register to the highway 49" (Col. 7, lines 37-42 – emphasis added).

However, merely disclosing that a substantially continuous sequential transfer of data is performed by applying a read strobe to the RAM buffers, where each RAM buffer contains a word of data, and where the word is output from each RAM buffer as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest "synchronously reading data from all of the two-port memories only when all of the two-port memories have data stored therein, thereby forming synchronous read data" (emphasis added), as claimed by appellant.

Appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above.

Issue # 7:

The Examiner has rejected Claim 18 under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5,765,186), in view of Stolowitz (U.S. Patent No. 6,018,778), and further in view of Yamamoto (U.S. Patent No. 5,801,859).

Group #1: Claim 18

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #6, Group #2.

In view of the remarks set forth hereinabove, all of the independent claims are deemed allowable, along with any claims depending therefrom.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP486).

Respectfully submitted,

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